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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 019516/0189

In re patent application of
SOMANATHAR et al
Serial No. 08/675,304
Filed: July 1, 1996
For: MOTION CONTROLLER ARCHITECTURE

Group Art Unit: 2317
Examiner: M. Meky

REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The instant Request for Reconsideration is being submitted in response to the Office Action mailed November 15, 1996 and December 16, 1996. Claims 23, 25-32 and 34 are pending in the application and are submitted for reconsideration.

Claims 23, 25, 27-32 and 34 were provisionally rejected under the 35 U.S.C. § 101 as claiming the same invention as claims 1 and 4 of copending Application Serial No. 08/673,317. This double patenting rejection is respectfully traversed.

This double patenting rejection is clearly inappropriate because claims 23, 25, 27-32 and 34 of the instant application can be literally infringed without literally infringing either claim 1 or 4 of the copending application. Claim 1 of the copending application recites:

> 1. A servo loop control apparatus comprising:
>
> input circuitry arranged to receive signals from a servo loop to be controlled;
>
> output circuitry arranged to provide signals to a servo loop to be controlled;
>
> a master processor to control said apparatus, said master processor being connected via a bus to a memory and having write access at any time to any location in a first portion of said memory and read access at any time to any location in said first portion and a second portion of said memory; and

> a second processor, said second processor communicatively coupled to at least one of said input and said output circuitry and programmed to operate autonomously of said master processor, said second processor being dedicated to specific, pre-programmed servo loop control tasks and being connected to said memory with write access at any time to any location in said second portion of said memory and read access to any location in said first and second portions of said memory, said second processor comprises means for executing repetitive preprogrammed servo loop processing instructions without interruption, thereby maintaining operation of a servo loop independent of said master program; and
>
> a plurality of vector registers, said vector registers forming a means for interrupting said servo loop processing in said second processor under a limited set of predefined conditions;
>
> wherein said at least one of said input circuitry and said output circuitry are controlled by said master processor and said second processor through said memory.

and claim 4 recites:

> 4. The apparatus recited in claim 1, further comprising an instruction RAM for access by said second processor, said instruction RAM storing instructions for user defined servo control loop routines.

Claims 23, 25, 27-32 and 34 of the instant application do not define identical subject matter as claim 1 or 4 of the copending application. Therefore, it is respectfully requested that the rejection under 35 U.S.C. § 101 be withdrawn.

Claims 25-27, 29-32 and 34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Haendler. The Office Action states that Haendler "inherently teaches that each processor would write preprocessed data to a portion (memory block) of the shared memory to be accessed by another processor, i.e., each processor would have read and write accesses to its portion of memory, and other processor(s) would have only read access to that portion of the memory."

This rejection is respectfully traversed, because the memory structure described in Haendler does not inherently contain the memory structure claimed in the instant application. As an example, the Examiner is directed to the attached illustration which may be representative of the memory structure described in Haendler.

In the illustration, processor #1 and processor #2 share memory 1/2 and processor #2 and processor #3 share memory 2/3 and so forth. After having finished assigned tasks, each processor transfers data into a block of memory which is shared by a processor coming next in the chain. Thus, processor #1 transfers data to memory 1/2 for use by processor #2; processor #2 transfers data to memory 2/3 for use by processor #3; and so forth. In the illustrated structure, there is no requirement that processor #1 be able to read from memory 1/2 in addition to being able to write to it. Similarly, there is no requirement that processor #2 be able to read from memory 2/3 in addition to being able to write to it.

In view of the foregoing, it is respectfully requested that the rejection under 35 U.S.C. § 102(b) over Haendler be withdrawn.

This application is now in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

March 17, 1997
Date

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